REMARKS.

This is a full and timely response to the outstanding nonfinal Office Action mailed June 20, 2001. Reconsideration and allowance of the application and presently pending claims, as amended, are respectfully requested.

Applicants acknowledge receipt of the prior art made of record but not relied upon in the instant Office Action. It is believed that this prior art does not affect the patentability of the present invention.

Upon entry of the amendments in this response, claims 1-10 and 17-20 remain pending in the present application. More specifically, claims 1 and 17 are directly amended and claim 19 has been canceled. These amendments are more specifically described herein. It is believe that the foregoing amendments and additions add no new matter to the present application.

Claims 1-5 and 17-20 have been rejected under 35 USC §103(a) as being unpatentable over Applicants prior art FIGs. 1 and 2. The Office Action asserts that FIGs. 1 and 2 of the present application disclose a first port 10', 11', 12' and 13' for outputting a signal; a second port 14, 15, 16 and 17 for receiving the signal; and an alignment link 30, 31, 32 and 33 for electrically connecting the first port with the second port; and the alignment link comprises a signal buffer for buffering a signal traveling along the alignment link between the first port and the second port.

Independent claims 1 and 17 have now been amended herein as noted above. These claims have been specifically amended to specify, among other things, a common area comprising an alignment link for electrically connecting said first port with said second port. Further, the first port extends directly into the common area from a first area, and, the second port extends directly into the common area from a second area.

The prior art shown in FIGs. 1 and 2 does not disclose or otherwise suggest an integrated circuit such as that specified by claims 1-10 and 17-20 herein. FIG. 2 herein, shows that first ports 10, 11, 12 and 13 extend from a first area 1 into a linking area 25. Bridging traces 20, 21, 22 and 23 are connected to the ports 10, 11, 12 and 13. These ports do not extend directly from the first area one into a common area as required by amended claims 1 and 17 herein.

As for claims 2-5 and 18-20, it is believed that the amendments herein to independent claims 1 and 17, as discussed above, sufficiently further distinguish these

claims over the prior art. In view of this, it is believed that dependent claims 2-5 and 18-20 are also allowable over the prior art.

Claims 6-10 have been rejected under 35 USC §103(a) as being unpatentable over the prior art FIGs. 1 and 2 in the present application, in view of *Mizuno, et al.* (USP 6,140,686). With regard to claims 6 and 7, the Office Action notes that Applicants prior art FIGs. 1 and 2 fail to disclose integrated circuit real estate comprising multi-levels. The Office Action asserts that *Mizuno, et al.* discloses an integrated circuit (FIGs. 1, 21 and Abstract) comprising multi-levels wherein the multi-levels comprises semiconductor level and a wiring level, the semiconductor levels form a buffer and control circuit so that the frequency of the oscillation output corresponds to the frequency of the clock signal (Abstract) and the wiring levels 110, 111, 112, 113 provide the power supply voltage to the circuit block 300 (FIG. 1). The Office Action asserts that it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the integrated circuits of Applicants prior art FIGs. 1 and 2 so that the integrated circuit real estate comprises multi-levels to maintain the frequency of the signal from the clock to the oscillation output and provide the power supply voltage to the circuit block shown by *Mizuno, et al.* Independent claim 1 has been amended herein as noted above. Each and every limitation of claim 1, as amended herein, must be considered in determining the patentability of claims 6-10. In view of the amendments to claim 1 discussed above, Applicants respectfully submit that dependent claims 6-10 herein are allowable over the prior art. Reconsideration and allowance of these claims is respectfully requested.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the now pending claims 1-10 and 17-20 are in condition for allowance. Favorable re-consideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 738-2378.

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Docket No. 050816-1460

Respectfully submitted,

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ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

The following is a marked up version of the amended claims, wherein bracketing denotes deletions and underlining denotes additions.

1. (Once Amended) An integrated circuit comprising:

a first port for outputting a signal;

a second port for receiving said signal;

a common area comprising an alignment link for electrically connecting said first port with said second port;[and]

said first port extends directly into said common area from a first area;

said second port extends directly into said common area from a second area; and

said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port.

17. (Once Amended) An integrated circuit comprising:

a first port for outputting a signal;

a second port for receiving said signal;[and]

a common area comprising an alignment means for electrically connecting said first port with said second port[.];

said first port extends directly into said common area from a first area; and

said second port extends directly into said common area from a second area.